I claim:

1. An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections;

a plurality of output ports, each output port operatively associated with a plurality of data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units for delivery to their associated output ports and, if the backlog reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

2. The ATM switch according to claim 1, wherein each of the data units designates a priority and the additional data units which designate relatively high priorities are not in violation of the rate limitation.

3. The ATM switch according to claim 1, wherein each of the data units designates a priority and the additional data units which designate relatively low priorities are in violation of the rate limitation.

4. The ATM switch according to claim 1, wherein each of the data units designates a priority and the determination of whether the additional data units which designate relatively low priorities are in violation of the rate limitation is based on a "leaky bucket" algorithm.

5. The ATM switch according to claim 1, wherein if the backlog falls below a particular level, the output controls are arranged to lift the rate limitation.

6. The ATM switch according to claim 1, wherein the data buffers are ~~physically associated with input ports~~.

7. The ATM switch according to claim 1, wherein the data buffers are physically associated with output ports.

8. The ATM switch according to claim 1, wherein the rate limitation is enforced at inputs.

9. The ATM switch according to claim 1, wherein the rate limitation is enforced at outputs.

10. An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections;

a plurality of output ports, each output port operatively associated with a plurality of data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units for delivery to their associated output ports and, if the backlog buffered in one or more selected stores reaches a particular level, to a enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

11. The ATM switch according to claim 10, wherein each data store buffers data units having a distinct priority.

12. The ATM switch according to claim 10, wherein each data store buffers data units having a distinct priority and input port combination.

13. The ATM switch according to claim 10, wherein each of the data units designates a priority and the additional data units which designate relatively high priorities are not in violation of the rate limitation.

14. The ATM switch according to claim 10, wherein each of the additional data units designates a priority and the additional data units which designate relatively low priorities are in violation of the rate limitation.

15. The ATM switch according to claim 10, wherein each of the data units designates a priority and the determination of whether the additional data units which designate relatively low priorities are in violation of the rate limitation is based on a "leaky bucket" algorithm.

16. The ATM switch according to claim 10, wherein if the backlog falls below a particular level, the output controls are arranged to lift the rate limitation.

17. The ATM switch according to claim 10, wherein the data buffers are physically associated with input ports.

18. The ATM switch according to claim 10, wherein the data buffers are physically associated with output ports.

19. The ATM switch according to claim 10, wherein the rate limitation is enforced at inputs.

20. The ATM switch according to claim 10, wherein the rate limitation is enforced at outputs.

21. The ATM switch according to claim 10, wherein each of the data units designates a priority and an input port and the determination of whether the additional data units which designate relatively low priorities and a particular input port are in violation of the rate limitation is based on a "leaky bucket" algorithm.

22. The ATM switch according to claim 21, wherein the particular input port is associated with a selected store whose backlog caused the selective filtering condition to be imposed.

23. A DIBOC-based ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections, each input port physically associated with a plurality of data stores and an input control for transmitting "Requests" to release data units;

a plurality of output ports, each output port operatively associated with a plurality of the data stores and physically associated with an output control for monitoring "Requests" to release data units; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units for delivery to their associated output ports, through information transmitted in "Requests" and, if the backlog reaches a particular level, to enforce a rate

limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

24. The ATM switch according to claim 23, wherein each data store buffers data units having a distinct priority.

25. The ATM switch according to claim 23, wherein each of the data units designates a priority and the additional data units which designate relatively high priorities are not in violation of the rate limitation.

26. The ATM switch according to claim 23, wherein each of the data units designates a priority and the additional data units which designate relatively low priorities are in violation of the rate limitation.

27. The ATM switch according to claim 23, wherein each of the data units designates a priority and the determination of whether the additional data units which designate relatively low priorities are in violation of the rate limitation is based on a "leaky bucket" algorithm.

28. The ATM switch according to claim 23, wherein if the backlog falls below the particular level, the output controls are arranged to lift the rate limitation.

29. The ATM switch according to claim 23, wherein the output controls impose the rate limitation by transmitting congestion control signals to the input controls.

30. The ATM switch according to claim 28, wherein the output controls lift the rate limitation by transmitting congestion control signals to the input controls.

31. The ATM switch according to claim 23, wherein each of the data units designates a priority and an input port and the determination of whether the additional

data units which designate relatively low priorities and a particular input port are in violation of the rate limitation is based on a "leaky bucket" algorithm.

32. The ATM switch according to claim 31, wherein the particular input port is associated with a selected store whose backlog caused the rate limitation to be imposed.